REMARKS

Claims 1-9 and 11-15 are pending in the application. Claims 1, 5 and 8 have been amended and claim 15 has been added by the foregoing amendment.

Applicant appreciates the Supervising Patent Examiner's offer to instruct the Examiner to grant an interview to the undersigned to discuss the application prior to examination of the concurrently filed Request for Continuing Examination (RCE). Consequently, the undersigned eagerly await a communication from the Examiner to schedule the interview.

Claims 1-9 and 11-14 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 6,338,078 ("Chang").

Exemplary embodiments are directed to a method for controlling the order of datagrams being processed by at least one processing engine. As recited in amended claim 1 for example, the at least one processing engine includes at least one input port and at least one output port, wherein each datagram or each group of datagrams has a ticket associated therewith by a ticket dispenser. Processors in the processing engine, once they become available, take a next ticket from the ticket dispenser and use it to control the order of the datagram or group of datagrams at the at least one input port of the processing engine and at the at least one output port of the processing engine.

Chang discloses a network in which inbound packets are distributed for processing over multiple CPUs. Chang provides multiprocessor scalability while maintaining packet order. As illustrated in Figure 3, Chang discloses a plurality of queues 62, 64, 66, 68 each corresponding to one of a plurality of CPUs 54, 56, 58 and 60 (reference numerals 50, 52, 54 and 56 are used in

duplicate). Every inbound packet is distributed into a queue. This is achieved by hashing each of the media access control (MAC) addresses of the inbound packets into the plurality of queues. As a result; packets associated with a given device (given MAC address) will be handled in the same queue. When one of the queues is started, one of the threads is scheduled to process packets on this queue. When all of the packets on the queue are processed, the thread becomes dormant.

As highlighted previously, in an extreme case, this would mean that if all packets have the same MAC address they would all go into the same queue and be handled by one CPU while the other CPUs remain idle.

While recognizing that Change fails to disclose a ticket dispenser, the Office Action asserts erroneously that Chang discloses a queuing mechanism for queuing the packets in such a way that packets arrive at the device driver in a certain sequence and are aligned in sequence to be processed by multiple processors. Chang merely discloses distributing packets across a number of CPUs (queues) to exploit the increased processing power of a multi-processor system. As each queue is associated with a CPU, each packet is processed in turn from the queue. Once the CPU has finished processing the packets in the queue assigned to that CPU, it will become idle until more packets are put into that queue.

The Office Action appears to suggest that the queuing mechanism of Chang allows processing of the packets in sequence between the CPUs with a central queuing mechanism (comprising a plurality of queues) and a single sequence of packets. This would require each CPU to scan all the queues of Chang to find the next packet in the sequence as there is no ticket

dispenser disclosed or suggested by Chang. As clearly disclosed by Chang, packets enter a queue using a hashing algorithm to achieve fair distribution across the queues and hence processors (each queue being associated with a single processor). There is no suggestion or teaching in Chang to enable one of ordinary skill in the art to arrive at a ticket dispenser mechanism as claimed.

The Office Action (on page 3) states that it would have been obvious to replace a ticket dispenser with a queuing system without any basis in Chang that would enable one of ordinary skill in the art to make such modification/substitution.

In fact, it is submitted that the ticket dispenser teaches away from the queuing system of Chang. Exemplary embodiments are directed to keeping the processors busy at all times. Chang is concerned with maintaining packet order. The packets (in Chang) are assigned to queues and corresponding CPUs in a deterministic way outside the control of the processor, in order to preserve the order of the packets. In exemplary embodiments, the processors decide when they need another packet and retrieve it via the ticket dispenser. Therefore, packet allocation is under the control of the processors and nondeterministic (i.e., out of order).

Based on the erroneous interpretation that Chang uses tickets, the Office Action appears to assume that these notional tickets are taken by waiting packets. However, as recited in claim 1, it is the processor that takes the next available ticket (and hence the next available packet) when they are free. Contrary to the assertions in paragraph 17 of the Office Action, Chang does not disclose the processor taking the next packet when it becomes available. The processors in Chang are given the next packet in their queue. The processors have no control over this (i.e.

being given the next packet in the queue) and hence no choice as to their next task. In exemplary embodiments, as recited in claim 7 for example, the processors can leave and not take a tickets (and hence a waiting packet) and proceed with some other processing task.

At least for these reasons, it is believed that claims 1, 5 and 8 are allowable over the teachings of Chang. The remaining claims (i.e. claims 2-4, 6, 7, 9 and 11-15), all of which depend on one of allowable independent claims 1, 5 and 8 are also allowable.

All of the rejections having been overcome, it is believed that this application is in condition for allowance and a notice to that effect is earnestly solicited. Applicant requests that the Examiner contact the undersigned at the number listed below.

Respectfully submitted,

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